WHAT IS CLAIMED IS:

1. A multiplication unit comprising:

a partitionable multiplier structure partitionable into two or more sub-tree structures,

the multiplication unit responsive to an indication of a first instruction type to be partitioned into the two or more sub-trees structure to perform multiple multiplication operations in parallel, and

responsive to an indication of a second instruction type to configure the sub-tree structures into a single data flow to perform a single multiplication operation.

2. The multiplication unit as recited in claim 1 wherein the first instruction type is a single instruction multiple data (SIMD) instruction and the second instruction is a non-SIMD instruction.

3. The multiplication unit as recited in claim 2 wherein the SIMD and non-SIMD multiplication operations include at least one of floating point and integer multiplication.

4. The multiplication unit as recited in claim 1 further comprising:

an input format stage coupled to receive one or more first input operands and to format the one or more first input operands according to a type of multiply operation being performed;

an encoder circuit coupled to receive the one or more formatted first input operands and supply control signals to multiplexer circuits used in generating partial products in the partitioned sub-tree structure; and

wherein the input format stage formats bits corresponding to edges of each partitionable sub-tree structure according to the instruction type specifying the multiply operation being performed.

5. The multiplication unit as recited in claim 4 wherein the formatted bits are formatted to be one of, identical to an adjacent bit, zero, or sign extended according to the instruction type.

6. The multiplication unit as recited in claim 4 wherein each partitioned sub-tree comprises:

a storage location storing a second input operand;

first selector circuits coupled to the storage location supplying the second input operand according to control signals received from the encoder circuit;

a plurality of adder circuits coupled in a tree structure and coupled to receive portions of partial products encoded according to the encoding circuit; and

second selector circuits coupled to particular portions of the sub-trees to select outputs from the sub-trees according the instruction type.

7. The multiplication unit as recited in claim 6 wherein each storage location is capable of storing an independent second input operand for SIMD operations.

8. The multiplication unit as recited in claim 1 wherein the multiplication unit is included on a processor.

9. A method of performing a multiplication operation using a partitionable data flow structure having a plurality of sub-trees comprising:

formatting one or more first operands by formatting at least a least significant bit in each data partition, each data partition corresponding to a sub-tree, that is adjacent to another data partition, according to an instruction decode;

supplying a second operand to each sub-tree of the partitionable multiplier structure; and

supplying the formatted one or more first operands to generate control signals for encoding the second operands to provide partial products supplied in each sub-tree.

10. The method as recited in claim 9 wherein the partitionable data flow structure functions as a single tree structure when the instruction decode specifies a non-SIMD multiplication operation and as a partitioned tree structure when the instruction decode specifies a SIMD instruction.

11. The method as recited in claim 9 wherein the second operand supplied to each sub-tree is the same second operand.

12. The method as recited in claim 9 wherein the second operand supplied to each sub-tree is a different second operand.

13. The method as recited in claim 9 further comprising selecting outputs from different locations in the sub-trees according to the instruction decode to form the multiplication result.

14. The method as recited in claim 9 wherein the formatted least significant bit is formatted to be one of, identical to a bit in an adjacent data partition, zero, or sign extended according to the instruction type.

15. The method as recited in claim 9 further comprising selectively performing one multiplication operation for a non-SIMD instruction in the partitionable data flow structure and performing at least two multiplication operation simultaneously in the partitionable tree structure for SIMD instructions.

16. The method as recited in claim 10 wherein the SIMD and non-SIMD multiplication operations include at least one of floating point and integer multiplication.

17. The method as recited in claim 10 wherein the encoding utilized is Booth encoding.

18. A method for performing multiplication operations comprising:

configuring a partitionable tree structure to be a single tree structure in response to a first multiplication instruction decode and as a partitioned

tree structure in response to a second multiplication instruction decode; and

performing at least two multiplication operations in parallel in the partitioned tree structure in response to the second multiplication instruction decode and performing a single multiplication operation in the partitionable tree structure in response to the first multiplication instruction decode.

19. The method as recited in claim 18 wherein the first multiplication instruction decode is a non-SIMD instruction and the second multiplication instruction decode is a SIMD instruction.

20. The method as recited in claim 19 further comprising formatting a Booth operand according to the instruction decode to prevent data associated with a sub-tree from corrupting a neighboring sub-tree when the partitionable tree structure is partitioned in response to the SIMD instruction decode.

21. The method as recited in claim 20 wherein a bit supplied to a Booth encoder at a boundary of a sub-tree is set to zero when the partitionable tree structure is partitioned for a SIMD instruction and for a non-SIMD instruction takes on a data value utilized by a neighboring sub-tree.

22. The method as recited in claim 20 further comprising providing a register in each sub-tree for the non-booth operand.

23. A apparatus for performing multiplication operations comprising:

means for configuring a partitionable tree structure to be a unified tree structure in response to a non-SIMD instruction decode and as a partitioned tree structure in response to a SIMD instruction decode; and

means for formatting data supplied to a booth encoder according to whether the instruction decode is a non-SIMD or SIMD instruction decode.